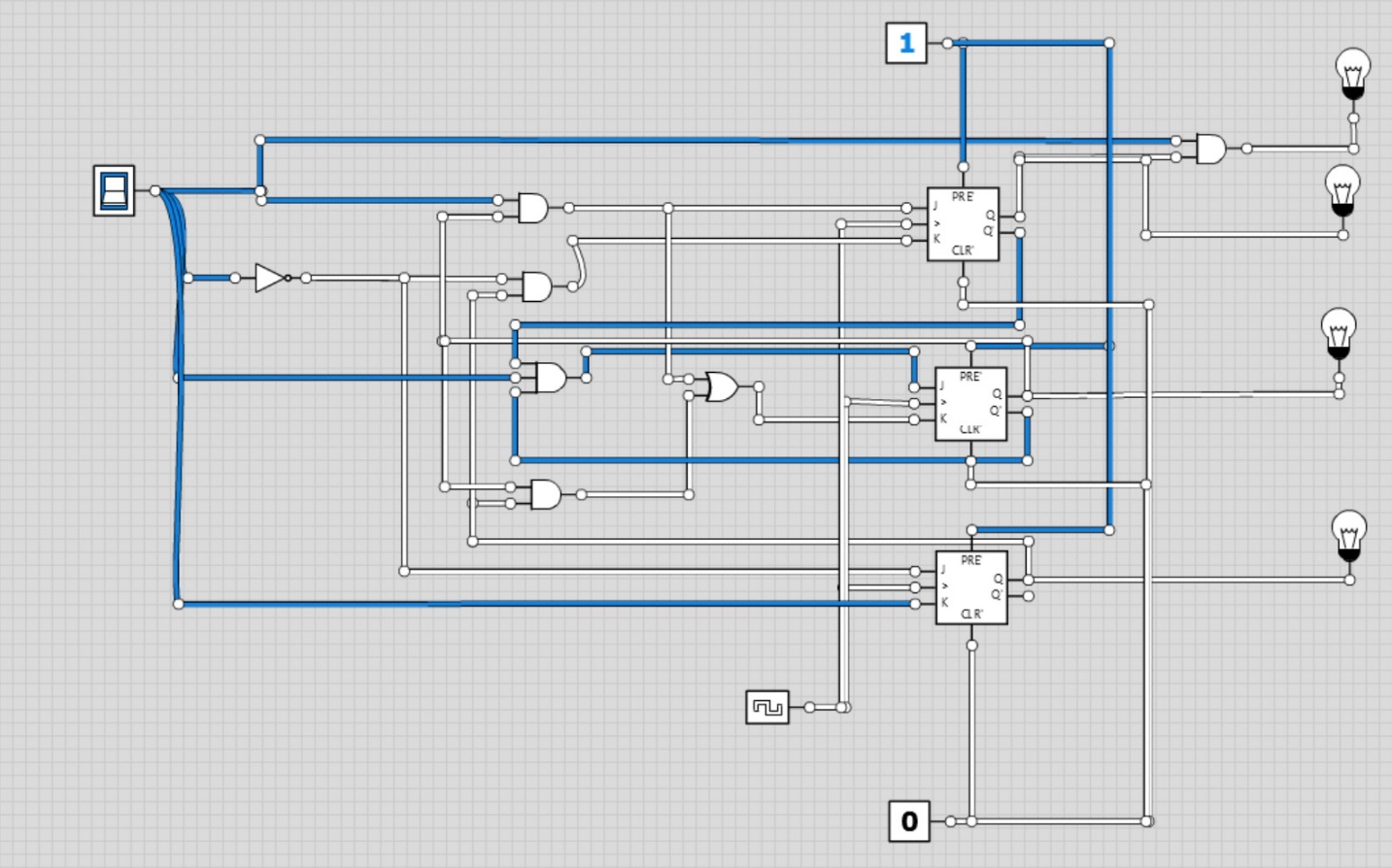
1)

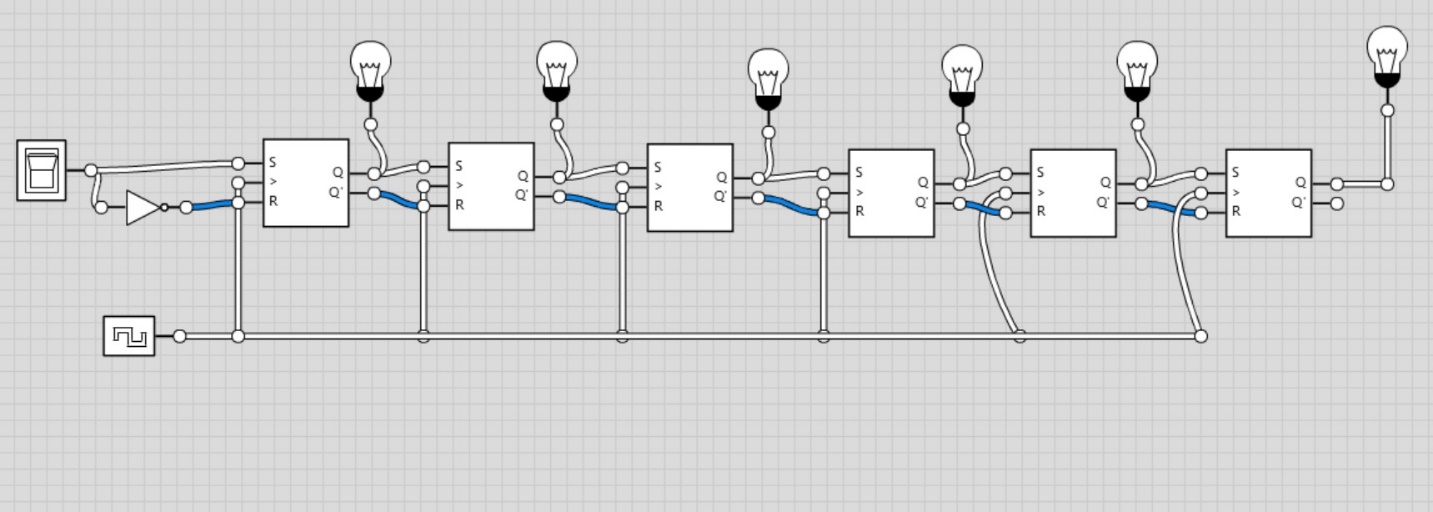


For this circuit the output is consistently 0 for all inputs

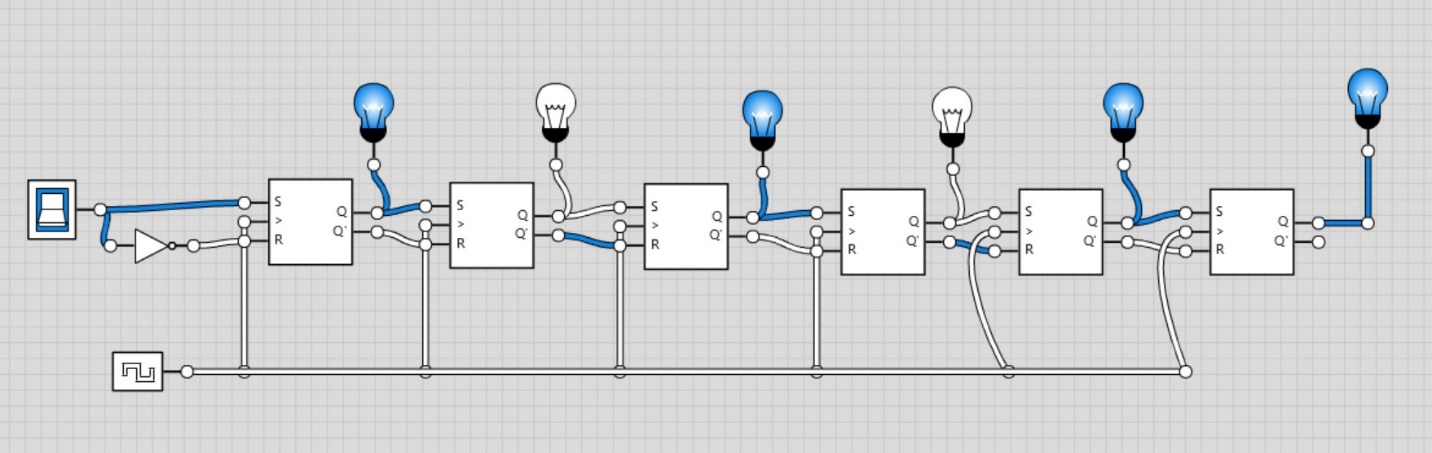
2)

Below is my circuit and the different states it was in as the shift register progressed

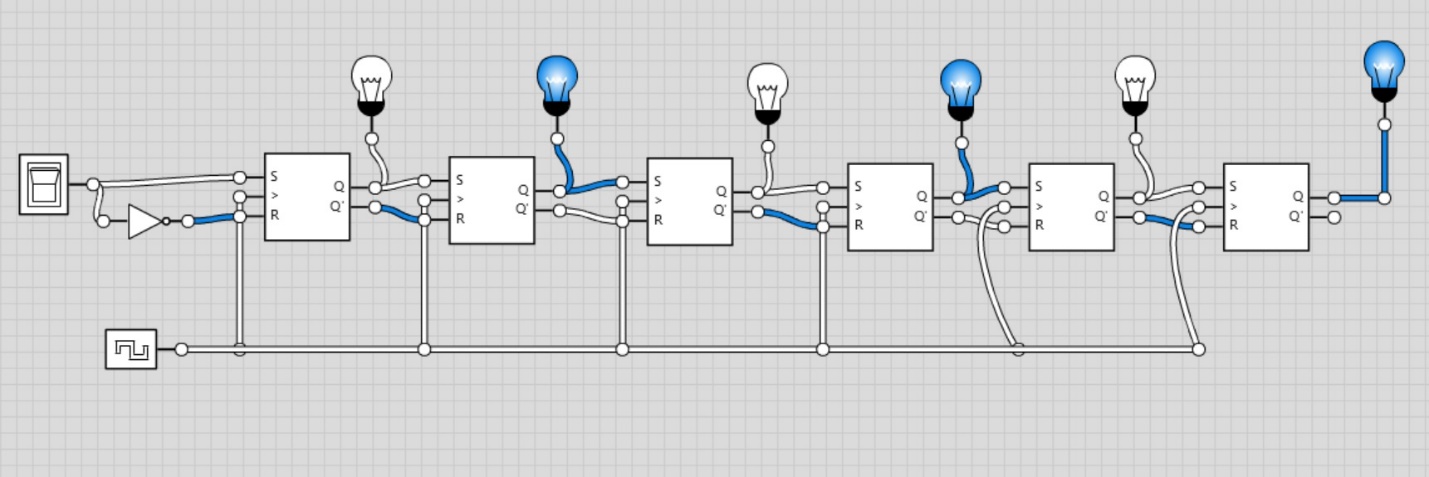
Default state



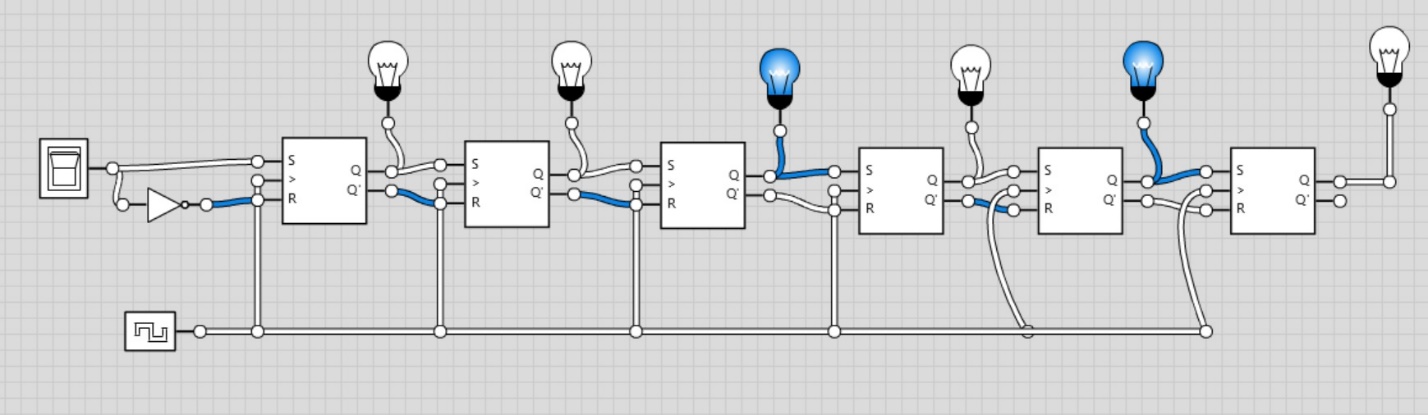
101011



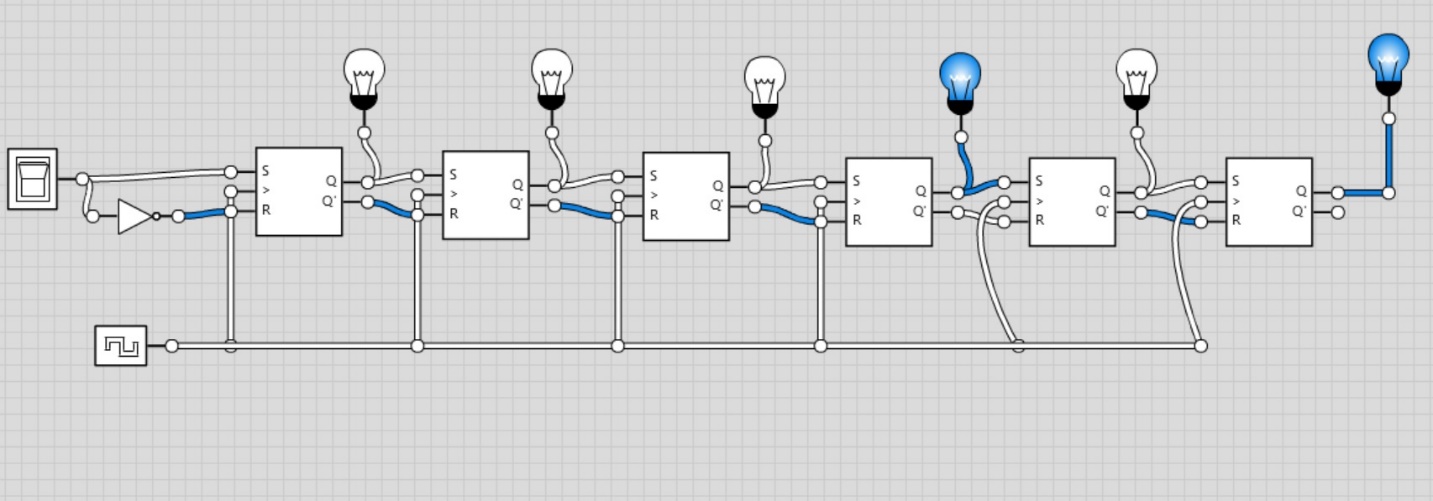
010101



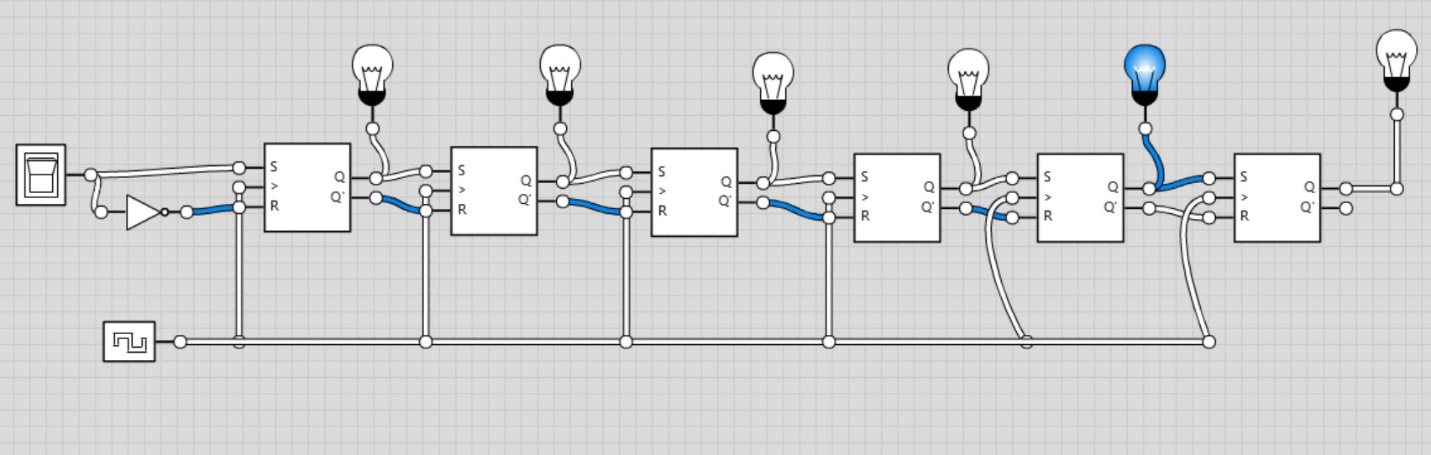
001010



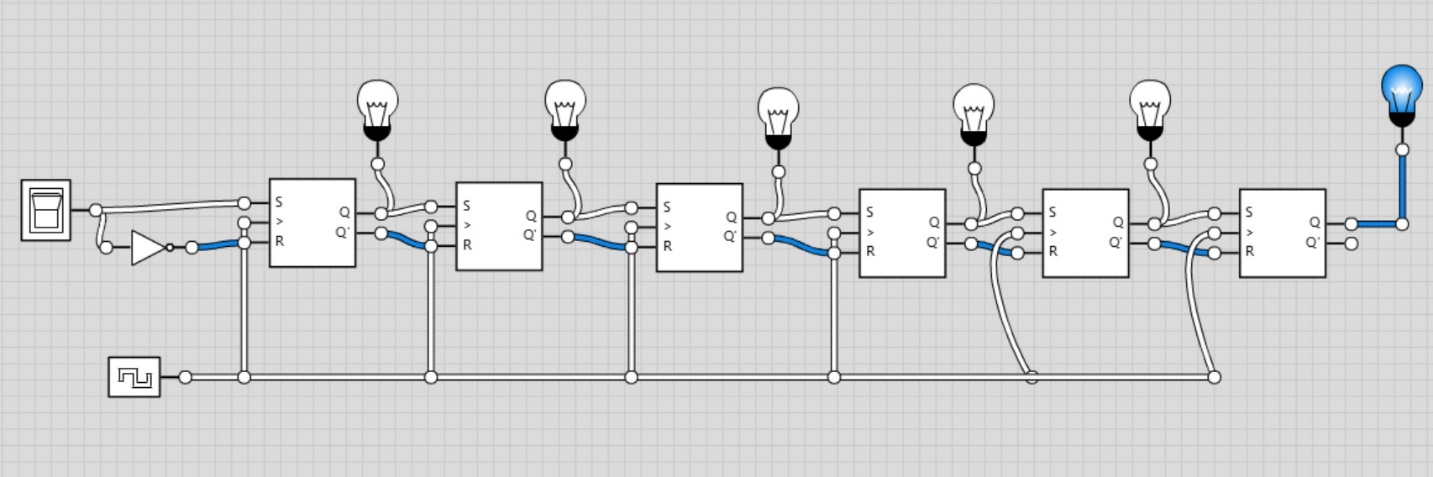
000101



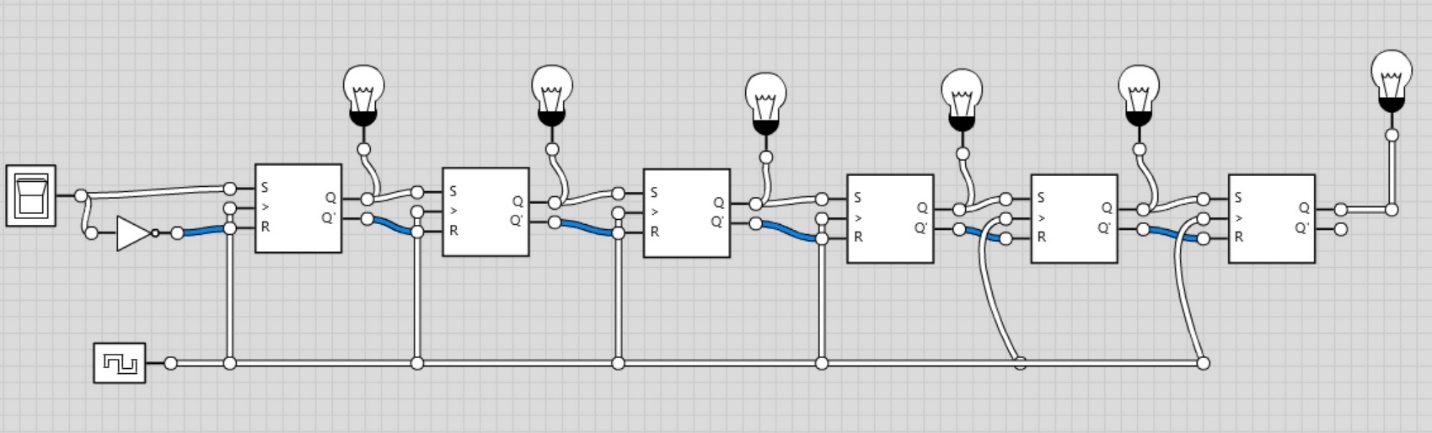
000010



000001



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Paper work:

